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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,766	02/03/2001	Chester A. Heath	296/1	7296

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EXAMINER	
PATEL, ASHOKKUMAR B	

ART UNIT	PAPER NUMBER
2154	5

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,766	HEATH ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Application Number 09/775, 766 was filed on 02/03/2001. Claims 1-18 are subject to examination.

Specification

2. Claims 6-12 are objected to because of the following informalities: These claims are presented as the dependent claims of claim 6. This seems to be an error. These claims are prosecuted as being the dependent claims of claim 5 for the purpose of this office action. Appropriate correction is required.

3. Claims 14 and 15 are objected because they are found to be identical. For the purpose of this office action they are being addressed as they are presented. Appropriate correction is required.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "over a network" in second line of the claim 16. It is unclear as to how the computer system as claimed as one system in independent claim 13 monitors and detects a fault state and transmits a reset signal to the host within the system, and the reset signal is sent over the network.

For purposes of this office action, they both will be treated as one. Appropriate correction is required

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 4 rejected under 35 U.S.C. 102(e) as being anticipated by Farmwald et al. (hereinafter Farmwald)(US 6, 598, 171).

Referring to claims 1 and 4,

The reference teaches the logic circuitry in a computer (Fig. 14, col.14, lines 65-67 and col.15, lines 1-14). The reference also teaches a protocol for master (primary computer) and slave (a computer or modular computer units) devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. (Abstract). These devices can be processing devices and CPUs. (col.5, lines 23-27, col.6, lines 9-15). The reference also teaches the reset procedure wherein the multiple reset commands issued by a primary computer (master) and by a device (a computer) which involves the logic circuitry inhibiting all but one reset command from resetting the device (a computer) at any one time. (col.14, lines 25-67 and col.15, lines 1-40).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 3 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farmwald et al. (hereinafter Farmwald)(US 6, 598, 171) in view of Broedner et al. (hereinafter Broedner)(US 5,793,993).

Referring to claims 2, 3, 5 and 6,

The reference Farmwald teaches a power on/off signal line originating from primary computer (col.6, lines 29-33). The reference also teaches decode modules which interpret commands received from primary computer. (col. 6, lines 54-58). The reference also teaches programmable registers which assume a prescribed state in response to interpreted commands and power on/off signal line. (col.6, lines 29-65). The reference fails to explicitly teach one or more AND gates which output a signal indicative of the status of decode module and programmable register and one or more OR gates which applies a reset signal to components of the computer, in response to the status of AND gate, programmable and power on/off line. The reference Broedner teaches the method of transmitting bus commands and one or more AND gates which output a signal indicative of the status of the inputting bus interface integrated circuit. The reference also teaches one or more OR gates which applies the signal in

response to the status of AND gate. The reference also teaches an explicit line (MBICINT) inputting the signal to OR gate. (Fig. 9, elements 902, 903, 901, col.35, lines15-34). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify Farmwald to include Broedner's the logic circuitry, as it is, in the computer providing the interface between the computer registers and decode modules such that the reset signal can be applied to the components of the computer by the output of the OR gate in response to the status of AND gate. This allows bus lines for carrying substantially all address, data and control information needed by the devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, the bus carries device-select information without the need for separate device-select lines connected directly to individual devices as taught by Farmwald.

Referring to claim 7,

The reference Farmwald teaches the claimed invention by stating that a protocol for master (primary computer) and slave (a computer or modular computer units) devices communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. (Abstract). These devices can be processing devices and CPUs. (col.5, lines 23-27, col.6, lines 9-15). Also, the reference teaches that the system includes one memory device connected in parallel to the bus, thus the devices (modular computer units) are connected through a common shared memory. (col.3, lines 41-52).

Referring to claim 8,

The reference Farmwald teaches the claimed invention. (col.5, lines 27-29).

Referring to claims 9-12,

The reference Farmwald teaches the claimed invention. (col. 14, lines 35-67 and col.15, lines 1-67 and col.16, 1-9).

9. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farmwald et al. (hereinafter Farmwald)(US 6, 598, 171) in view of Horst et al. (hereinafter Horst)(US 6, 496, 940).

Referring to claim 13,

The reference Farmwald teaches the logic circuitry in a computer (Fig. 14, col.14, lines 65-67 and col.15, lines 1-14). The reference also teaches a protocol for master (host computer) and slave (client computers) devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. (Abstract). These devices can be processing devices and CPUs. (col.5, lines 23-27, col.6, lines 9-15). The reference also teaches the reset procedure wherein the multiple reset commands issued by a primary computer (host computer) and by a device (a computer) which involves the logic circuitry inhibiting all but one reset command from resetting the device (a computer) at any one time. (col.14, lines 25-67 and col.15, lines 1-40). The reference also teaches that a CPU can include both slave and master functions depending on the mode of operation and the state of the system. (col. 6, lines 4-19). The reference fails to explicitly teach a circuitry for monitoring and detecting a fault state. The reference Horst teaches the fault

detection as being the responsibility of the hardware (circuitry for monitoring and detecting a fault state. (col.2, lines 37-44). The reference also teaches a multiprocessing system in which each processor has the capability of checking on the operability of it's sibling processors (plural client computers and a host computer), and taking over the processing of a processor found or believed to have failed. (col.6, lines 13-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify Farmwald (wherein a computer can include both client and host functions depending on the mode of operation and the state of the system), in addition, to include the capability of Horst's processor where each processor (computer) in the system can check on the operability of it's sibling processors (plural client computers and a host computer) to detect the fault which can be reset by Farmwald's computer's capability. This allows reduction in power consumption and increases system reliability as taught by Farmwald.

Referring to claims 14 and 15,

The reference Farmwald teaches the circuitry for detecting includes circuitry for monitoring a clocking signal by the master configuration. (col.18, lines 58-67 and col.19, lines 1-28).

Referring to claim 16,

The reference Farmwald teaches the system where multiple devices can be Masters (computer driving the configuration). Therefore, it teaches that the signal can be received from any of the monitoring source other than the faulty host indicating a fault with the host.

Referring to claims 17 and 18,

Keeping in mind the teachings of Farmwald, Farmwald fails to explicitly teach the detecting circuitry including circuitry for executing a diagnostic software program and configuring client computer as a host computer in response to detecting a fault with the host computer. The reference Horst teaches the fault detection as being the responsibility of the hardware (circuitry for monitoring and detecting a fault state and fault recovery as being the responsibility of the software. (col.2, lines 37-44). The reference also teaches a multiprocessing system in which each processor has the capability of checking on the operability of it's sibling processors (plural client computers and a host computer), and taking over the processing of a processor found or believed to have failed (configuring client computer as a host computer in response to detecting a fault with the host computer). (col.6, lines 13-17). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to modify Farmwald (wherein a computer can include both client and host functions depending on the mode of operation and the state of the system), in addition, to include the capability of Horst's processor where each processor (computer) in the system can check on the operability of it's sibling processors (plural client computers and a host computer) to detect the fault by executing the software (diagnostic software program) and which can be reset, if necessary, by Farmwald's computer's capability. This increases system reliability as taught by Farmwald.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (703) 305-2655. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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